CLAIMS

We claim:

1. A programmable logic device comprising:

input/output buffers adapted to programmably support a plurality of signal types;

a serializer deserializer circuit adapted to receive a serial input data stream and extract a clock and provide a parallel data output signal and further adapted to receive a parallel data input signal and provide a serial output data stream; and

a programmable interconnect adapted to selectively couple the input/output buffers to the serializer deserializer circuit.

2. The programmable logic device of Claim 1, wherein the programmable interconnect couples the input/output buffers to the serializer deserializer circuit to route signals through the serializer deserializer circuit when the signals exceed a clock rate of a core logic of the programmable logic device, and decouples the input/output buffers from the serializer deserializer circuit to bypass the serializer deserializer circuit when the signals are within the clock rate of the core logic.

3. The programmable logic device of Claim 1, wherein the signal types include LVTTL, LVCMOS, PCI, PCI-X, SSTL, HSTL, GTL+, CTT, BLVDS, LVDS, and LVPECL.

4. The programmable logic device of Claim 1, wherein the serializer deserializer circuit comprises:

a first receiver having a deserializer and a clock and data recovery function;

a first transmitter, associated with the first receiver, having a serializer function;

a second receiver having a deserializer and a clock and data recovery function; and

a second transmitter, associated with the second receiver, having a serializer function.

5. The programmable logic device of Claim 4, wherein the serializer deserializer circuit further comprises a phase-locked loop circuit adapted to provide a high speed clock for the serializer deserializer circuit.

6. The programmable logic device of Claim 5, wherein the programmable interconnect couples the input/output buffers to the serializer deserializer circuit when high speed serial data transfer capability is required over differential signal input/output paths.

7. The programmable logic device of Claim 1, further comprising a memory, the programmable interconnect selectively couples the memory to the input/output buffers.

8. The programmable logic device of Claim 7, wherein the memory provides synchronization support.

9. The programmable logic device of Claim 7, wherein the memory comprises RAM, ROM, FIFO, single-port, or dual-port memory.

10. A programmable interface circuit, within a programmable logic device, comprising:

input/output buffers adapted to support a number of input/output signal types;

means for providing serializer/deserializer and clock and data recovery; and

means for programmably coupling the providing means to the input/output buffers for high-speed serial signal streams transferred through the input/output buffers which exceed a core clock rate of the programmable logic device.

11. The programmable interface circuit of Claim 10, wherein the input/output signal types include single-ended signals and differential signals.

12. The programmable interface circuit of Claim 10, further comprising a memory, wherein the coupling means programmably couples the memory to the input/output buffers to provide synchronization functions.

13. The programmable interface circuit of Claim 12, wherein the coupling means decouples the providing means from the input/output buffers and routes signals transferred through the input/output buffers between the input/output buffers and the memory or a core logic of the programmable logic device when a rate of the signals is within the core clock rate.

14. The programmable interface circuit of Claim 13, wherein the core logic implements logic, memory, arithmetic, or register functions.

15. The programmable interface circuit of Claim 10, wherein the providing means comprises a pair of serializer deserializer circuits and a phase-locked loop.

16. The programmable interface circuit of Claim 10, wherein the coupling means comprises a pair of input/output blocks and a switch matrix.

17. A method of providing a programmable interface for a programmable logic device, the method comprising:

providing buffers adapted to programmably transfer a number of different signal types to and from the programmable logic device; and

providing a programmable interconnect to selectively couple or decouple an interface circuit, having serializer,

deserializer, and clock and data recovery capability, to the buffers depending upon the signal type.

18. The method of Claim 17, wherein the signal types comprise single-ended signals and differential signals.

19. The method of Claim 18, wherein the programmable interconnect couples the interface circuit to the buffers when the signal type is a differential signal that exceeds a core clock rate of the programmable logic device, and decouples the interface circuit when the signal type does not exceed the core clock rate.

20. The method of Claim 19, further comprising providing memory adapted to programmably couple to the programmable interconnect.